

Operation and Installation Manual

Niagara NT 944 iHX
Industrial Single Board Computer

for Pentium, MMX, 75-233MHz
supporting AMD K6 up to 350MHz

November 29, 1998
Revision 1.0



Niagara SMD Technology Inc
304 Carlingview Drive
Toronto, Ontario M9W 5G2
Canada

Phone: (416) 675-2366
Fax: (416) 675-4242
Website: www.niagaratech.com

1.0 INTRODUCTION

The Niagara NT944 iHX single board computer is a high reliability design for the Intel MMX and non-MMX processors, supporting speed ranges from 75-233MHz. AMD and Cyrix are supported as well up to 350MHz. The board provides support for three PCI bus mastering slots on the corresponding backplane and one slave. A multi I/O controller provides serial, parallel, floppy and dual FAST ATA/IDE (also called Enhanced) interfaces. An optional SCSI controller for Ultra wide interface is designed-in and available on demand (model=NT944s-iHX). Due to the heat generated by the processor, it is recommended that this board be configured, on setup, with a CPU fan and heatsink cooler, either directly on top of the CPU, or a minimum height 1.5" heatsink on the CPU and a fan blowing directly against the heatsink. To prevent potential dust contamination and subsequent failure, it is advised to clean the fan periodically. We recommend double ball bearing or sintered sleeve bearing fans for added reliability.

SPECIFICATIONS:

- The Niagara NT944 iHX is constructed on ten layers with a split power plane to support single and split plane voltage processors. (Non-MMX and MMX). It supports power regulation for all current processors with a unique switching power design to minimize heat dissipation to help keep the processor cool. Ample decoupling capacitors, both ceramic and tantalum, smooth out any voltage spikes and keep the NT944 iHX well within specifications for nominal voltage.
- The NT944 iHX operates at 66MHz Bus and all rated CPU speeds for Pentium class processors from 75MHz to 233MHz for Intel and 350MHz for AMD.
- Memory configurations of up to 256MB with 2 banks of two modules each per bank SIMM DRAM (minimum 8Mb). Automatic BIOS RAM configuration.
- 512KB of synchronous Burst/Pipelined cache soldered on the board.
- Supports 1 floppy port, 1 parallel port and 2 serial (16550 UART) ports. IrDA (InfraRed), USB (Universal Serial Bus) port, PS/2 mouse port and a DIN AT keyboard. All standard I/O ports use shrouded casings.
- AWARD BIOS, stored in EPROM flash. Battery backed setup with replaceable Dallas RTC chip.

The NT944 iHX system board is designed with the 82439HX PCI-bus based chip-set. It provides increased system integration for PCI-bus IDE interface and USB from the chip-set by way of a header, but also uses a fast multi I/O chip design for serial, floppy and parallel interface which supports ECP and EPP protocols. In addition a single IrDA port is provided.

All ISA and PCI expansion slots are made with nickel plated phosphorous bronze material. The CPU and memory sockets are made of beryllium copper. All gold contacts are of 70micron of gold to provide a minimum of 500 insertion without degradation of continuity. And finally, care must be taken when inserting CPU and memory modules into associated slots or expansion sockets to avoid damaging circuits on the board.

The NT944 iHX supports four 72-pin SIMM memory modules in two banks to make up a 64-bit memory bus. The smallest module must be 4Mb each of either parity or non-parity, or EDO architecture. To get an affective error correcting scheme using EDO memory a single chip of 8K size can be installed beside the cache tag RAM. The speed recommended on all memory is 60ns.

The NT944 iHX supports two PCI connectors, one enhanced (primary) and one standard, for four IDE devices and detects IDE hard disk types and size through the BIOS auto-detect utility.

An optional SCSI controller using the Adaptec 7880 chip-set provides Ultra wide and narrow interface on the board.

An extensive watchdog design provides for power-fail warning and can be addressed in hardware and software.

Last, but not least, the Niagara NT944 iHX board uses over 500 capacitors, ceramic and tantalum, to provide stability of signal quality, maintaining strict control on capacitance, over-undershoots, crosstalk and other deterrents to operational quality.

Every board is pre-tested and burned-in for 72 hours.

2.0 UNPACKING

CAUTION, unless the following precautions are followed, the manufacturer cannot be held responsible for any resulting damages. The motherboard contains static-sensitive devices that can be damaged or destroyed by rough or improper handling. Use caution when touching the card, handle by the edges only. Do not touch connectors or chips. Do not remove the board from the protective bag unless you are wearing a wrist strap designed for static discharge and connected to ground.

Proceed with the following steps:

- Examine the cardboard container for any signs of external damage.
- Open the cardboard container.
- Cut the seal of the protective bag.
- Remove the board from the bag.
- Place the bag on a flat surface and the board on top.
- Examine the board for signs of damage.
- If necessary, fill out a damage report and forward copies to your supplier indicating shipping particulars.

Note: Hold the board by edges only, since there are sharp pins which could cause injury to your fingers and hands.

Do not flex or bend the board in any manner, as this may damage the PCB traces and/or surface mount component solder joints.

3.0 INSTALLATION

3.1 SYSTEM DEFAULT SETTINGS

CPU Clock	233 MHz
Cache RAM	Synchronous 512KB
Multi I/O Controller	Enabled
Printer ECP Mode	DMA 3
Printer port, LPT1	IRQ 7
Serial COM 1	IRQ 4
Serial COM 2	IRQ 3
PS/2 Mouse	IRQ 12
IDE Channel 1	IRQ 14
IDE Channel 2	IRQ 15

3.2 QUICK INSTALLATION

Step 1

LOCATE PIN 1 ON THE CABLES YOU ARE GOING TO USE.

When attaching the internal bus cables to the on-board host adapters and the peripherals, make sure that pin 1 is maintained throughout the bus. Pin 1 is denoted on most grey ribbon cables by a red stripe. On the Niagara NT944 iHX system board pin 1, on all headers, is located towards the CPU socket. Check your peripheral's manual for the correct pin 1 orientation.

Step 2

CONNECT ONE END OF THE CABLE TO THE INTERNAL HEADERS.

Line up pin 1 on the cables to pin 1 on the internal header connectors for all peripheral connections to be made. Firmly, but in a straight forward fashion, as to avoid bending the pins of the internal connector, put the cable end on to the connectors, lining up pin 1 associations.

Step 3

ATTACH FREE END OF CABLE TO THE DEVICES.

If tangled, untangle the cables so they will lie freely within the cabinet when the system case cover is replaced. Install the disks or other devices as specified in the manufacturer's directions. Make sure the pin 1 orientation is maintained.

Step 4

INSERT CPU.

Make sure to maintain pin 1 orientation of the CPU to the socket, which is located on the right top towards the edge of the board. Carefully lift the handle of the "ZIF" socket up and gently insert the Pentium chip into the socket. Press socket handle down until it locks.

Note: For CPUs with a single voltage (eg. non-MMX processors) close all three jumpers on JP21, open all on JP23. For CPUs with split voltage (eg. MMX processors) do the reverse: close all jumpers on JP21, open all on JP23.

Step 5

SET CPU SPEED

Set speed of CPU using jumpers on tables 1.1 - 3.2. (See Appendix)

Check for and set jumpers on JP22 for clock multiplier rate.

Set JP24 and JP5 to match Voltages for Core and I/O for Intel, AMD or Cyrix and JP 21, 23 as per tables 1.1 - 3.2.

Also watch processor specific jumper settings J33 and J32 for AMD only.

Step 6

INSERT MEMORY

First, align each module on angle down into the keyed slot, then rotate against the centre until the metal latches lock.

Memory Bank 0 is made up of the bottom two sockets, J13, J14. Memory Bank 1 are the top sockets J15, J16.

Please note that unlike the cables, Pin 1 is located in the direction of the chipset opposite to the cable orientation.

4.0 CONFIGURATION

SYSTEM MEMORY CONFIGURATION

The NT944 iHX supports different sizes of memory on each of the two banks. One bank (64-bit wide) is made up with 2 connectors. Different type and size of memory cannot be mixed in one bank. Architecture supported is 1M, 2M, 4M, 8M, 16M, 64M, 128M x 36 bit with parity, or 32-bit fast page mode (without parity), as is Extended Data Out (EDO). When using EDO memory adding an 8Kb memory chip in socket U27, memory controller allows 1-bit ECC memory operation. No jumper is needed for any configuration. It is recommended that gold plated memory modules be used to assure error-free mating to gold memory sockets.

CACHE MEMORY CONFIGURATION

L2 (Level 2) cache uses 512KB of synchronous pipelined/burst cache memory which is soldered on the board.

BIOS SETUP

The Award BIOS provides a built-in Set-up program which allows the user to modify basic system configurations and hardware parameters. The modified data will be stored in a battery backed CMOS RAM so data will be retained when power is turned off. The information stays unchanged unless there is a configuration change in the system, such as hard drive replacement or other peripheral equipment.

TO ENTER SETUP PROGRAM

Power on the computer and press key immediately, this will bring you into the BIOS CMOS SETUP UTILITY.

The menu displays all the major selection items and allows the user to select any one choice. The selection is made by moving the cursor key to the item and press <Enter>. An on-line help message is displayed at the bottom of the screen. When a selection is made the menu of selected item will appear so the user can modify selected configuration parameters.

BIOS FEATURES SETUP

Selecting the BIOS FEATURES SETUP option in the CMOS SETUP UTILITY menu allows the user to change system related parameters in the displayed menu. This menu shows all of the NT944 iHX default values as set at the factory or other installation facility. Again the user can move the cursor by pressing direction keys and <PgDn> or <PgUp> keys to exchange the parameters. This setup program provides two convenient ways to load the factory default parameters from BIOS, if shown data is corrupted. This allows the system to recover from any possible error.

CHIP-SET FEATURES SETUP

Choose this menu and with the <F6> key reload initial values after any hardware changes or other system changes.

POWER MANAGEMENT SETUP

This menu allows the user to modify power management functions of CPU and Multi I/O chip. In general these parameters should not be changed unless setup data is corrupted.

PCI CONFIGURATION SETUP

This program allows the user to modify PCI IRQ signals when various PCI cards are added to the PCI slots

5.0 CHANNELS MAP: TIME / DMA / INTERRUPT / MEMORY/ IO

5.1 TIME MAP

Channel 0	System timer interrupt
Channel 1	DRAM refresh request
Channel 2	Speaker tone generator

5.2 DMA CHANNELS

<u>Channel</u>	<u>Description</u>
0	Available
1	On board ECP option
2	Floppy disk
3	On board ECP (*Default)
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

5.3 INTERRUPT MAP

NMI: Parity check error

<u>IRQ</u>	<u>Description</u>
0	System Timer interrupt from TIMER 0
1	Keyboard output buffer full
2	Cascade for IRQ 8-15
3	Serial port 2
4	Serial port 1
5	Parallel port 2
6	Floppy disk drive
7	Parallel port 1
8	RTC clock (Real Time Clock)
9	Available
10	Available
11	Available
12	PS/2 mouse
13	Math coprocessor
14	Onboard Hard disk (IDE 1) channel
15	Onboard Hard disk (IDE 2) channel

5.4 MEMORY MAP

<u>Address Range</u>	<u>Size</u>	<u>Description</u>
00000-7FFFF	512K	Conventional memory
80000-9FBFF	127K	Extended Conventional memory
9FC00-9FFFF	1K	Extended BIOS data area if PS/2 mouse is installed
A0000-C7FFF	160K	Available for High DOS memory
C8000-DFFFF	96K	Available for High DOS memory and adapter ROMs
E0000-EEFFF	60K	Available for USB
EF000-EFFFF	4K	Video Service Routine for Monochrome and CGA adapter
F0000-F7FFF	32K	BIOS CMOS setup utility
F8000-FCFFF	20K	BIOS runtime service routine (2)
FD000-FDFFF	4K	Plug and Play ESCD data area
FE000-FFFFF	8K	BIOS runtime service routine (1)

5.5 I/O MAP

Range	Description
000-01F	DMA controller (Master)
020-021	Interrupt Controller (Master)
022-023	I/O ports Chip-set control registers
040-05F	Timer control registers
060-06F	Keyboard interface controller (8042)
070-07F	RTC ports & CMOS I/O ports
080-09F	DMA register
0A0-0BF	Interrupt controller (Slave)
0C0-0DF	DMA controller (Slave)
0F0-0FF	Math coprocessor
1F0-1F8	Hard disk controller
278-27F	Parallel port LPT 2
2B0-2DF	Graphics adapter controller
2F8-2FF	Serial port COM 2
360-36F	Network ports
378-38F	Parallel port LPT1
3B0-3BF	Monochrome & Parallel port adapter
3C0-3CF	EGA adapter
3D0-3DF	CGA adapter
3F0-3F7	Floppy disk controller
3F8-3FF	Serial port COM1

6.0 ON BOARD PERIPHERALS

The Niagara NT944 iHX motherboard is using a Multi I/O chip which has power management features and supports the following controller functions: Two serial ports with NS16550 compatible UARTS, 16-bit FIFO, modem control circuitry and optional PS/2 type mouse port logic. One parallel port with multi protocol P1284 compatible interface, supporting standard and bidirectional protocol, ECP (Extended Parallel Port), ESP (Enhanced Parallel Port) with a 128-byte FIFO, capable of up to 2Mbyte/sec transfer rates. A 4Mbyte floppy disk controller using a digital data separator with data rates to 1Mbyte/seconds and support all sizes of floppies up to 2.88Mbyte. And finally an IDE interface for embedded drives with primary and secondary IDE address port selects

6.1 SERIAL PORTS

The Niagara 944 iHX supports two built-in serial communication ports. The generic device used in this design uses a 16-bit FIFO UART and is fully register compatible with the NS16C550. The chip is driven with a clock frequency of 1.8462 MHz and supports speeds up to 56 Kbaud.

The following EIA RS-232 signals are supported:

- CTS : (Clear to Send):** This is a modem control signal. The control process can read this signal by reading bit 4 of the modem status register found in the 452 chip. Bit 0 of the same register will indicate if the CTS signal has changed since the previous reading. If the interruption jumper is installed and the interrupts are enabled, each time that the CTS signal changes an interrupt is generated.
- DSR (Data Set Ready):** This is a signal used by the modem to indicate that it is ready to initiate a transmission. The signal can be read by accessing bit 5 of the modem status register. Bit 1 of the same register indicates that the signal changed since the previous reading. The change of this signal can also, if properly configured, generate interrupts.
- DCD (Data Carrier Detect):** When this signal is low, it indicates to the controller that a data set detected a data carrier. This signal is found in bit 7 of the modem register, and bit 3 indicates if it changed from the last reading. A change of status in this signal can produce an interrupt if properly configured.
- RNG (Ring Indication):** When low, it indicates that the modem or data set detected a telephone ringing signal. The status of the signal is stored in bit 6 of the modem register. Bit 3 indicates that the signal changed since the previous reading. Like the previous signals, an interrupt is also available.
- DTR (Data Terminal Ready):** When active (low) indicates the modem that the controller is ready to communicate. By writing to the bit 0 of the modem control register the signal can be set to low or high as required.
- RTS (Request To Send):** If low, informs the modem that the controller is ready to send data. By programming the modem control register this signal can be set to high or low level as required.
- TX (Transmit Data):** This signal is used to transmit the serial data from the controller to the serial device in use.

6.2 PARALLEL PORT

The Niagara NT944 iHX system board has a single built-in bidirectional parallel port, which supports the Centronics interface

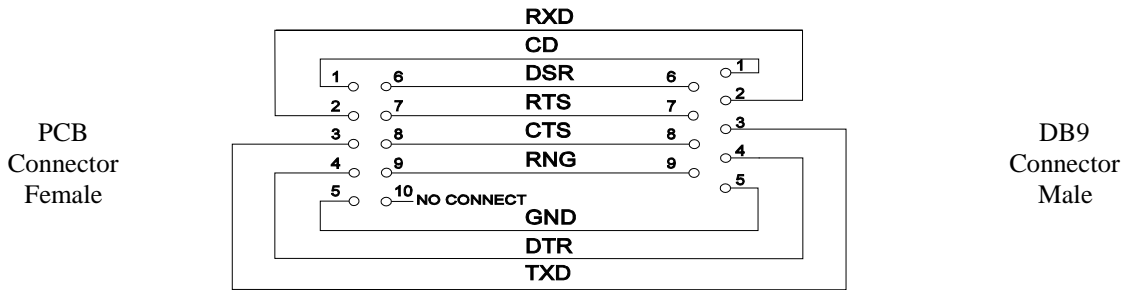
The parallel port circuitry is contained in the multi I/O device. Another application of the parallel port can be a bi-directional connection used by software to transfer files between two systems.

PARALLEL PORT SIGNALS:

STROBE -	A 0.5 microsecond minimum, high, active pulse clocks data into the printer. Valid data must be present for a minimum 0.5 microseconds before and after the strobe pulse.
AUTO FD XT -	A logical 1 causes the printer to line-feed after a line is printed.
INIT -	A logical 0 starts the printer (50 microsecond pulse, minimum)
SLCT IN -	A logical 1 selects the printer.
D0-D7 -	Data bus.
ERROR -	A logical 0 means the printer has encountered an error condition.
SLCT -	A logical 1 means the printer is selected.
PE -	A logical 1 means the printer has selected the end of paper.
ACK -	This line represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready for to accept another. Normally this signal will be active for approximately 5 microseconds before BUSY stops.
BUSY -	When this signal is active, the printer is busy and cannot accept data. It may become active during data entry, while the printer is off-line, during printing, when the printhead is changing positions or while an error state.

6.3 INTERNAL CABLES

6.3.1 SCHEMATIC DRAWING - DB9 Serial Cable



NOTES:

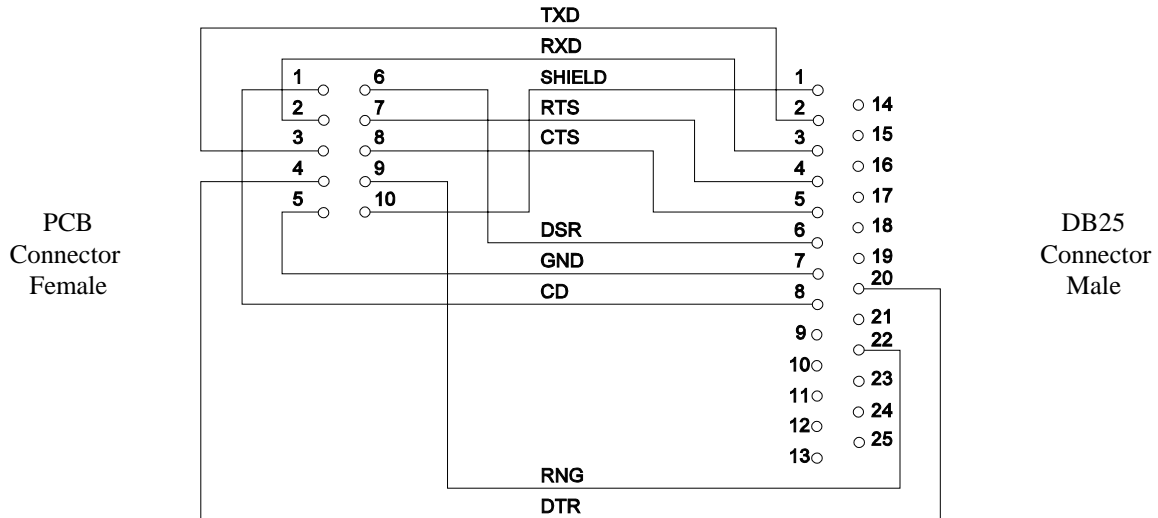
- PCB connector pin-out is the same as that of the header assembly on the motherboard for J12 and J13, when looking from the top. See illustration.
- A straight forward way to make a cable requires:
 - 9 wire ribbon Cable
 - 10 pin (or 2 rows of 5 pins) ribbon cable insulation displacement connector (e.g. MOLEX 39-51-2104)
 - DB9 flat cable insulation displacement connector (e.g. CINCH FC-09).

When pressing 10 pin connector, line up pin 1 with the red marking on the 9 wire flat cable. Similarly for the DB9 connector, line up pin 1 with the red marking on the flat cable.

- The DB9 connector is IBM compatible as outlined in the document "Personal Computer AT Serial / Parallel Adapter".
- Standard RS232 voltage level:

ON :	+3V to +15V
OFF :	-3V to -15V
INVALID:	ALL OTHERS

6.3.2 SCHEMATIC DRAWING - DB25 Serial Cable



NOTES:

- PCB Connector pin-out is the same as that of the header assembly on the motherboard for J12 and J13 when looking from the top. See illustration.
- PCB connector is a 10 pin (or 2 rows of 5 pins) ribbon cable insulation displacement connector
eg) MOLEX39-51-2104
- To make the cable requires crossing of wires in the DB 25 connector.
- The DB 25 connector is IBM compatible as outlined in the document:
IBM Asynchronous Communication Adapter.
- Standard RS232C voltage levels:

ON	+3V	to	+15V
OFF	- 3V	to	- 15V
INVALID	ALL OTHERS		

6.4 LOOPBACK PLUG: Serial Ports / Parallel Ports:

The standard connection of signals shown enables external loopback testing of such diagnostics software as:
Qaplus™ from Diagsoft
Checkit™ from Touch Stone Software

Serial Port Loopback:

Signals:

RXD	↔	TX
CTS	↔	RTS
DTR	↔	DSR , CD, RNG

DB9 (female) Implementation:

Connect pins 2 + 3
Connect pins 7 + 8
Connect pins 1 + 4 + 6

DB25 (female) Implementation:

Connect pins 2 + 3
Connect pins 4 + 5
Connect pins 20 + 6 + 8

Parallel Port Loopback:

Interface Standard Centronics
Loopback Status to Commands

DB45 (male):

Connect pins 1 + 13
Connect pins 2 + 15
Connect pins 10 + 16
Connect pins 11 + 17
Connect pins 12 + 14

APPENDIX A - BIOS

A.1 Recoverable POST Errors

Whenever a recoverable error occurs during the power on self test (POST), the system BIOS will display an error message describing the problem in sufficient detail so it can be corrected.

Two additional recoverable errors are audible rather than displayed. The audible error generated during POST is a long tone followed by two short tones. This audible error will result from either a failing video configuration (no card installed or faulty) or an invalid external ROM module that does not properly checksum to zero. Any other audible errors consisting of one long tone followed by a series of short tones will be from an external ROM module (e.g. VGA)

All codes can be displayed and output to Port 80H, and 8-bit POST diagnostic card.

A.2 BIOS Checkpoint Codes

During POST, the BIOS signals a checkpoint by outputting a code to I/O address 80H. This code can be used to establish how far the BIOS executed through the power on sequence and what test is currently being performed. This is done to help troubleshoot faulty system boards.

If the BIOS detects a terminal error condition it will halt the POST process and attempt to display the checkpoint code on the screen. The checkpoint code written to the screen will match the code written to port 80H. The code will be written repeatedly to the screen which may cause "hash" to some CGA systems.

If the system hangs before the BIOS detects the terminal error, the value at port BOG will be the last test performed. In this case, the terminal error cannot be displayed on screen

The following is a list of checkpoint codes which are written before their respective tests.

POST BIOS Codes

02	Reserved
04	Reserved
03	Initialize devices: DMA, 8259, 8254 controller, RTC chip
05	Keyboard controller test
06	Reserved
07	Verify CMOS's R/W functionality
C1	Auto-detection of on board DRAM and cache
C5	Copy BIOS from ROM into E0000-FFFFFF shadow RAM
08	Test the first 256K DRAM
09	Initialize cache
0A	Initialize 32 interrupt vectors to handlers, Identify CPU, Initialize Power Management
0B	Verify RTC, read CMOS data into BIOS stack area, assign I/O and Mem for PCI device
0C	Initialize data BIOS area
0D	Program chipset's value, measure CPU speed for display and initialize, set system speed
0E	Test video RAM, BIOS checksum
0F	8237 DMA controller, channel 0 test
10	DMA channel 1 test
11	DMA page register test
12-13	Reserved
14	8254 timer 0, Counter 2 test
15	Test 8259 interrupt mask bits for channel 1
16	Test 8259 interrupt mask bits for channel 2
17	Reserved
19	Test 8259 functionality
1A - 1D	Reserved
30	Detect base memory & Extended memory size
31	Test Base memory, test Extended memory
32	Program multi I/O chip according to setup
33-3B	Reserved

3C	Set flag for user to enter CMOS Setup Utility
3D	Initialize keyboard, install PS/2 mouse
3E-3F-40	Reserved
BF	Finalize chipset program
41	Initialize FD controller
42	Initialize HD controller
43	Initialize serial & parallel ports
44	Reserved
45	Initialize math coprocessor
46-4D	Reserved
4E	F1 key on errors, if any
4F	Password, if needed
50	Write CMOS value in the BIOS stack area back to CMOS
51	Reserved
52	Initialize all PCI ROMs, assign IRQ, PnP (IO, IRQ, DMA), program RAM parity,
61	Turn on Level 2 cache, power management, show system configuration
62	Program NumLock, typematic rate & speed from Setup
63	Update PnP ESCD information, clear memory, boot system via INT 19H
FF	System boots, pass control to operating system

All numeric entries are hexadecimal.

If error B0, B1 or 30 is detected by the BIOS, an additional word of information will be displayed to the screen and to port 80H. This word will reflect the bit or address line which failed. For example if "B0 0002" is displayed, address line 1 (represented by bit one) has failed. If "30 1020" is displayed, then data bits 12 and 5 have failed in the upper 16 bits.

The same information will be output to port 80H. The checkpoint code will be output followed by a delay, the high order byte, another delay, and then the low order byte of the error. This will be repeated continuously.

AWARD BIOS SETUP

The Award BIOS ROM has a built-in Setup program to allow user modification of basic system configuration. This type of information is stored in battery backed RAM (Dallas chip), so that it retains the Setup information when the power is turned off. We limit the explanation of the BIOS to a minimum and recommend that the user maintains the factory setup and only change values after a thorough understanding of implications of change. In case the system has been down and lost its BIOS memory always reload the original set-up values when prompted on the respective pages of the menus or sub-menus: Load Setup Default.

NOTE: The setup-menu has been optimized for this board to meet reliability criteria of registers and timing, only after extensive tests by Niagara engineers. Unless you are a qualified engineer and understand the items function and implication, we recommend strongly to always re-load BIOS set-up Defaults.

Entering Setup

Power on the computer. After the sign-on message of the video card and "Niagara" appears, press DEL immediately after being prompted on the screen, during the POST routine (Power On Self Test).

The Main Menu

Once you enter Award BIOS CMOS Setup Utility, the main menu will appear on the screen. Use arrow keys to navigate through the screen. Press enter to accept or select the sub-menu.

Standard CMOS Setup

Here you enter, when setting the board up for a first time, Date, Time, Hard drive Selection, Floppy drives, Video

BIOS Feature Setup

Default values from the factory are loaded. We offer a limited choice of changes for the users' convenience. System performance will not be affected.

Chip-set Features Setup

In this mode the user can and should change DRAM timing to match the memory in use. Once again we recommend to retain or load factory settings by using F6: Load Bios Defaults.

Power Management Setup

Changes can be made to Doze Mode, Standby Mode, Suspend Mode only when it is set to "User define".

Description of the Power Management mode selection:

A:	Disabled	The system operates in normal condition (Non-Green)
	Maximum Savings	This mode will maximize the power saving capability
	Minimum Savings	This mode will minimize the power savings capability
	User Define	Allows user to define timeout parameters to control power saving time. Refer to next section B:
B:	HDD Standby	Timer can be set from 1-15 minutes to shut hard drive down
	System Doze	Timer starts to count when no PM event occurs and can be set from 1 minute up to 1 hour
	System Standby	This timer starts to count when "System Doze" mode timer has timed out and no PM events occurred. Valid range is from 1 minute up to 1 hour.
	System Suspend	This function works only when the Pentium CPU is installed. The timer starts to count when "System Standby" mode timer has timed out and no "PM Events" occurred. Valid range from 1 minute up 1 hour.

Description of the "Green Functions"

HDD Standby

When system stops reading or writing to the Hard disk, the timer starts to count. The system will cut off the HDD power when timer runs off the set time. The system will not resume operation until either a read from or a write to HDD command is executed.

Doze

The system hardware will drop down CPU clock from normal working speed when timer timeout occurs.

Standby

In this mode the CPU will continue to work at slow speed. The screen will be blanked out.

Suspend

When mode is timed out the chip-set will suspend the CPU clock immediately. The power consumption is even lower than in standby mode. The screen is blanked out.

PM Events

There are 15 PM Events in the power management mode. The user can initialize any PM Events to be "Enable" or "Disable". When the system detects no activity on any of the enabled events, it will start the system "Doze" timer first. Then it will look at the "Standby" and start the countdown for it. On that timeout and other events remaining silent, the system will enter the Standby mode. By now the system will process the standby power savings procedures and start the system "Suspend" timer. Again, when this timer times out, the CPU clock will stop by dropping the system clock down to zero and will remain that way until any of the "Enable" events occur.

PCI Configuration Setup

When enabled the BIOS will depend on information provided by Plug and Play software (ICU) provided by the PCI card vendor in order to ensure that there are no conflicts with non PCI, (also called "Legacy") adapter cards. The ICU utility will update and save the information to the ESCD (Extend System Configuration Data).

When you have true PCI cards plugged into the system, you will not have to change anything in the SETUP program. When disabled, it is extremely important to verify the proper "Interrupt" settings to prevent system hangs.

APPENDIX B:

CONNECTORS

J3	PS/2 keyboard
J2	PS/2 mouse
J5	Serial port COM 2
J6	Serial port COM 1 (DB9)
J7	Floppy disk
J8	Parallel port LPT 1
J21	USB (not installed)
J22	USB (not installed)
J26	IrDA/IR (not installed)
J24	IDE1 Primary IDE
J23	IDE2 Secondary IDE
JP28	PC104 8-bit (not installed)
JP29	PC104 16-bit (not installed)
SJP3	50-pin SCSI (not installed)
SU9	69-pin SCSI (not installed)
J13,14	Memory bank 0
J15,16	Memory bank 1

APPENDIX C:

JUMPERS

JUMPER SETTINGS FOR INTEL, AMD, CYRIX PROCESSORS

Note: It may, at first, look a little unwieldy, but setting correct jumpers is easy. The reason for so many possibilities is simply that AMD and Cyrix assigned different pins and often different voltage from those processors made by Intel. We could have automated the settings exclusively for all Intel processors. But we wanted to provide flexibility of choice and exactly rated voltages, even for those other processors.

We recommend the following: First identify the CPU made by Intel, or AMD, or Cyrix. Then look for the Table in the Appendix (B) corresponding to the CPU: For Intel see Table 1.1 and 1.2. For AMD see Table 2.1 and 2.2. For Cyrix see Table 3.1 and 3.2. These charts define the speed and model, if non-MMX or MMX, the clock multiplier, the Core voltage and the I/O voltage. For AMD they even address specific pin assignments unique to AMD only. Mark the row for the corresponding CPU on each of the two Tables for future reference, find the double row of jumper JP 22 for the clock multiplier rate, you may need a maximum of 4 jumpers, depending on the CPU.

Next move to the other Table corresponding to the CPU, mark the row for your CPU, follow the row's instructions on setting of jumper JP 24 for the Core voltage setting, JP 5 for the I/O setting, and jumpers JP21, JP23, J33, J32.

JP 23	Power plane setting	
	Non-MMX processors	
	Pentium 75MHz-200 MHz	Jumper block open, when core voltage (VCore) and I/O voltage (VIO) <u>are the same</u>
	MMX processors	
	Pentium 166-266MHz	Jumper block closed, when core voltage (VCore) and I/O voltage (VIO) <u>are different</u>
JP22	Clock rate (Multiplier)	The CPU speed is determined by internal clock rate multiplied by a factor from 1.5 to 4.5 times. See Tables below: Note different Tables for Intel, AMD, Cyrix
J8	always on	
J21	(not used)	
J23	(not used)	
J26	(not used)	
J28	(not used)	
J29	(not used)	
J37	(not used)	
JP1	(not used)	
JP4	always on	
JP8	always on	
JP28	(not used)	
JP29	(not used)	
JP3	BIOS EPROM Select	Pin 1-2 is set for 5V Flash EPROM, *Default Pin 2-3 is set for 12V Flash EPROM
JP2	Clear CMOS	*Default = open, clears CMOS when closed
J27	Function connector	Top row: Ext SMI, Power Monitor, Speaker, Bottom row: Turbo LED, HD LED, Keylock
J36	Watchdog timer	Disabled: Jumper on Pin 1-2
J34	Power failure input	Default: no jumpers (CUSTOMER SPECIFIC)

APPENDIX C:

INTEL

Table 1.1

INTEL	V I/O [V]	VCORE [V]	CLK	RATE	JP22 (CLK/RATE)									
					pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 11-12	pin 13-14	pin 15-16		
	3.135-3.600													
Pentium - 75 P54C	(3.3) 3.3675	-----	50	1.5	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	
Pentium - 90 P54C	(3.3) 3.37	-----	60	1.5	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	
Pentium - 100 ? P54C	(3.3) 3.37	-----	50	2.0	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	
Pentium - 100 ? P54C	(3.3) 3.37	-----	66	1.5	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	
Pentium - 120 P54C	(3.3) 3.37	-----	60	2	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	
Pentium - 133 P54C	(3.3) 3.37	-----	66	2	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	
Pentium - 150 P54C	(3.3) 3.37	-----	60	2.5	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	
Pentium - 166 P54C	(3.3) 3.37	-----	66	2.5	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	
Pentium - 200 P54C	(3.3) 3.37	-----	66	3	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	
	3.135-3.600	2.700-2.900												
Pentium-166 (MMX) P55C	(3.3) 3.3675	(2.8) 2.8	66	2.5	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	
Pentium-200 (MMX) P55C	(3.3) 3.37	(2.8) 2.8	66	3	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	
Pentium-233 (MMX) P55C	(3.3) 3.37	(2.8) 2.8	66	3.5	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	

Table 1.2

INTEL	JP24 (VCORE)					JP5 (VIO)					JP21	JP23	J33	J32	
	pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	ALL	ALL	VCORE	GND	
													AMD	AMD	
Pentium - 75 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 90 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 100 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 120 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 133 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 150 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 166 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium - 200 P54C	OFF	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF	
Pentium-166 (MMX) P55C	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	
Pentium-200 (MMX) P55C	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	
Pentium-233 (MMX) P55C	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	

AMD

Table 2.1

AMD	V I/O [V]	VCORE [V]	CLK	RATE	JP22 (CLK/RATE/Y33;X34;W35)								
					pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 11-12	pin 13-14	pin 15-16	
	3.450-3.600												
AMD-5K86-P75 75MHz	(3.52) 3.525	-----	50	1.5	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
AMD-5K86-P90 90MHz	(3.52) 3.53	-----	60	1.5	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
AMD-5K86-P100 100MHz	(3.52) 3.53	-----	66	1.5	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
MODEL 0	3.450-3.600												
AMD-K5-PR75 75MHz	(3.52) 3.525	-----	50	1.5	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
AMD-K5-PR90 90MHz	(3.52) 3.53	-----	60	1.5	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
AMD-K5-PR100 100MHz	(3.52) 3.53	-----	66	1.5	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
MODEL 1	3.450-3.600												
AMD-K5-PR120 90MHz	(3.52) 3.525	-----	60	1.5	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
AMD-K5-PR133 100MHz	(3.52) 3.53	-----	66	1.5	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
MODEL 2	3.450-3.600												
AMD-K5-PR166 116MHz	(3.52) 3.525	-----	66	1.75	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
MODEL 6 MMX	3.135-3.600	2.755-3.045											
AMD-K6/166ALR	(3.3) 3.3675	(2.9) 3.045	66	2.5	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF
AMD-K6/200ALR	(3.3) 3.37	(2.9) 3.0	66	3	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
MODEL 6 MMX	3.135-3.600	3.1-3.3											
AMD-K6/233ANR	(3.3) 3.37	(3.2) 3.2	66	3.5	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
MODEL 7 MMX	3.135-3.600	2.100-2.300											
AMD-K6/200AFR	(3.3) 3.3675	(2.2) 2.2	66	3	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
AMD-K6/233AFR	(3.3) 3.37	(2.2) 2.2	66	3.5	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
AMD-K6/266AFR	(3.3) 3.37	(2.2) 2.2	66	4	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
AMD-K6/300AFR	(3.3) 3.37	(2.2) 2.2	66	4.5	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON
MODEL 8 MMX	3.135-3.600	2.100-2.300											
AMD-K6-2/233AFR	(3.3) 3.37	(2.2) 2.2	66	3.5	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
AMD-K6-2/266AFR	(3.3) 3.37	(2.2) 2.2	66	4	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
AMD-K6-2/300AFR	(3.3) 3.37	(2.2) 2.2	66	4.5	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON
AMD-K6-2/333AFR	(3.3) 3.37	(2.2) 2.2	66	5	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
AMD-K6-2/350AFR	(3.3) 3.37	(2.2) 2.2	66	5	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON

AMD

Table 2.2

AMD	JP24 (VCORE)					JP5 (VIO)					JP21	JP23	J33	J32
	pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	ALL	ALL	VCORE	GND
													AMD	AMD
AMD-5K86-P75 75MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
AMD-5K86-P90 90MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
AMD-5K86-P100 100MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
MODEL 0														
AMD-K5-PR75 75MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
AMD-K5-PR90 90MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
AMD-K5-PR100 100MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
MODEL 1														
AMD-K5-PR120 90MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
AMD-K5-PR133 100MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
MODEL 2														
AMD-K5-PR166 116MHz	ON	ON	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
MODEL 6 MMX														
AMD-K6/166ALR	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6/200ALR	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
MODEL 6 MMX														
AMD-K6/233ANR	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
MODEL 7 MMX														
AMD-K6/200AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6/233AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6/266AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6/300AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
MODEL 8 MMX														
AMD-K6-2/233AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6-2/266AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6-2/300AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6-2/333AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON
AMD-K6-2/350AFR	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON

CYRIX

Table 3.1

CYRIX		V I/O [V]	VCORE [V]	CLK	RATE	JP22							
						pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 11-12	pin 13-14	pin 15-16
		3.150-3.600											
6x86-P120+	100 MHz	(3.3) 3.3675	-----	50	2	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
6x86-P133+	110 MHz	(3.3) 3.37	-----	55	2	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
6x86-P150+	120 MHz	(3.3) 3.37	-----	60	2	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
6x86-P166+	133 MHz	(3.3) 3.37	-----	66	2	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
6x86-P200+	150 MHz	(3.3) 3.37	-----	75	2	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
		3.150-3.450	2.630-2.970										
6x86L-P150+	120 MHz	(3.3) 3.3	(2.8) 2.8	60	2	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
6x86L-P166+	133 MHz	(3.3) 3.3	(2.8) 2.8	66	2	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
6x86L-P200+	150 MHz	(3.3) 3.3	(2.8) 2.8	75	2	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
		3.135-3.465	2.800-3.000										
6x86 MX-PR200	166 Mhz	(3.3) 3.3	(2.9) 2.9	66	2.5	OFF	OFF	ON	ON	OFF	ON	OFF	OFF
6x86 MX-PR233	188 Mhz	(3.3) 3.3	(2.9) 2.9	75	2.5	ON	OFF	OFF	ON	OFF	ON	OFF	OFF
6x86 MX-PR233	200 Mhz	(3.3) 3.3	(2.9) 2.9	66	3.0	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
6x86 MX-PR266	225 Mhz	(3.3) 3.3	(2.9) 2.9	75	3.0	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86 MX-PR266	233 Mhz	(3.3) 3.3	(2.9) 2.9	66	3.5	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF

Table 3.2

CYRIX		JP24 (VCORE)					JP5 (VIO)					JP21	JP23	J33	J32
		pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	ALL	ALL	VCORE	GND
														AMD	AMD
6x86-P120+	100 MHz	ON	OFF	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
6x86-P133+	110 MHz	ON	OFF	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
6x86-P150+	120 MHz	ON	OFF	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
6x86-P166+	133 MHz	ON	OFF	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
6x86-P200+	150 MHz	ON	OFF	ON	ON	OFF	X	X	X	X	X	ON	OFF	OFF	OFF
6x86L-P150+	120 MHz	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86L-P166+	133 MHz	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86L-P200+	150 MHz	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86 MX-PR200	166 Mhz	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86 MX-PR233	188 Mhz	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86 MX-PR233	200 Mhz	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OPP	OFF	ON	OFF	OFF
6x86 MX-PR266	225 Mhz	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6x86 MX-PR266	233 Mhz	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF

APPENDIX D:

WATCHDOG TIMER J36

If a hardware failure occurs such that the system “hangs” due to any reason., a reset pulse is generated by the Watchdog timer circuit to restart the system.
The Watchdog feature is implemented onboard and can be activated in hardware or software.

(Please refer to the table below: where N = WATCHDOG TIMEOUT).

1. Hardware configurable Watchdog timer, J36: Pin pair 13, 14 and 15, 16

When this mode is selected, the Watchdog timer is always enabled and is serviced by the ALE signal. On failure to produce an ALE signal, a reset pulse is generated to reset the system. The table below shows a fixed hardware setting and subsequent software setup.

WATCHDOG TIMER SERVICE - HARDWARE STROBE.

The watchdog timer can be serviced by AEN (Address Enable) ISA-bus signal. Should the system crash due to any reason, a rest pulse will be generated to restart the system.

2. Software configurable Watchdog timer:

When activated in software it must be serviced by one I/O command: “ IO write with D0=1 to I/O location 201 (hex). Following a software reset, the Watchdog is always disabled.

ENABLE WATCHDOG TIMER.

The Watchdog timer is enabled once you write DO=1 to I/O address 201(hex).
Once it is enabled, it must be serviced every N milliseconds,
or reset pulse will be generated to restart the system.

WATCHDOG TIMER SERVICE - SOFTWARE STROBE.

This is done by reading I/O address 201h, once every N milliseconds, to verify proper software execution.

DISABLE WATCHDOG TIMER.

To disable the Watchdog timer function write: D0=0 to I/O address 201h

TABLE -- WATCHDOG TIMER CONFIGURATION
(AND POWERGOOD “PWRGOOD” THRESHOLD):

J34 Power failure input Default: no jumpers
J36 Watchdog timer Jumper on Pin 1-2 is set for default of 1milisecond

PWRGOOD THRESHOLD	WATCHDOG TIME-OUT N			J36 -- WATCHDOG JUMPER SETTING								WATCHDOG STROBE	COMMENT
	MIN	TYP	MAX	pin 1-2	pin 3-4	pin 5-6	pin 7-8	pin 9-10	pin 11-12	pin 13-14	pin 15-16		
[V]	[ms]	[ms]	[ms]										
4.65	1000	1600	2250	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	HARDWARE	
4.65	1000	1600	2250	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	SOFTWARE	
4.75	500	1200	2000	OFF	ON	ON	OFF	ON	ON	OFF	ON	SOFTWARE	
4.50	500	1200	2000	OFF	ON	ON	OFF	OFF	ON	OFF	ON	SOFTWARE	
4.75	250	600	1000	OFF	ON	OFF	OFF	ON	ON	OFF	ON	SOFTWARE	
4.50	250	600	1000	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	SOFTWARE	
4.75	62	150	250	OFF	ON	OFF	ON	ON	ON	OFF	ON	SOFTWARE	
4.50	62	150	250	OFF	ON	OFF	ON	OFF	ON	OFF	ON	SOFTWARE	
4.65	N/A	N/A	N/A	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	N/A	DEFAULT

APPENDIX E:

POWER FAILURE INPUT

The PFI (Power Failure Input) is a 1.25V threshold detector for power fail warnings of external devices. The PFI is compared to an internal 1.25V reference. If PFI is less than 1.25V IOCHK# signal goes low (active).

IOCHK# (I/O Channel Check - ISA-bus Signal)

An expansion board can assert IOCHK# to signal to the main CPU that a serious error has occurred. Assertion of IOCHK# causes an NMI (Non-Maskable Interrupt), if Port 061h bit 3 is set to "0" and NMI's are enabled.

Parity errors and uncorrectable system errors exemplify problems that might cause an expansion board to assert IOCHK#.

J34	Pin 1-2	Disable Power Failure Input.
	Pin 3-4	The external voltage divider drives PFI from PWR_MON (Power Monitor) header (on J27)
	Pin 5-6	On board voltage divider. The line is monitored by two user defined resistors at position R3 and R4. (R3 is connected to +5V, R4 to Ground). Select the ratio of R3 and R4 such that PFI sees 1.25V when +5V falls to its trip point - Vtrip. $(5-1.25) / R3 = (1.25 \text{ Vtrip}) / R4$

The PFI status is available by reading I/O address 201h bit 1.

If it reads 0, the circuit has detected a low power warning from PFI. If it reads 1, power is good.

Please contact our factory for circuit illustration and more detail.